Conversores A/D e D/A para chip de Smart Grid

Design House

chipus

Cliente (direto)

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

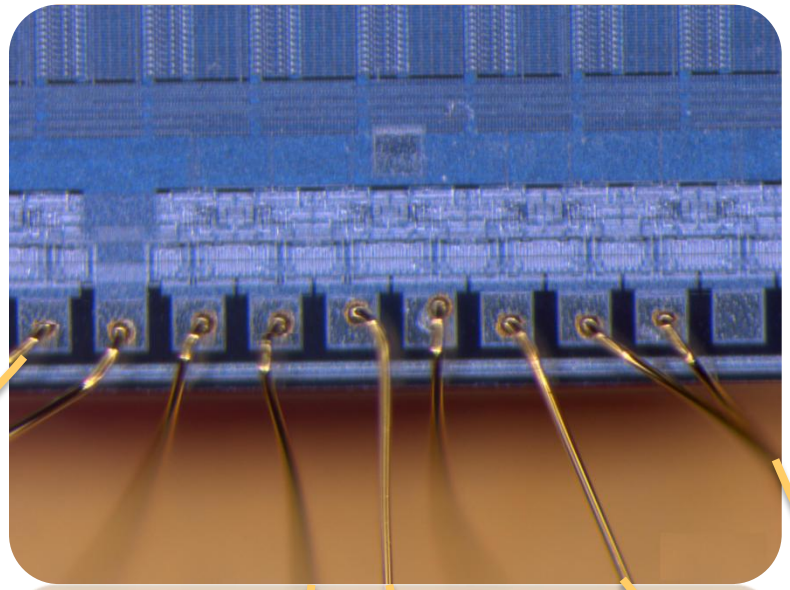
Electronics Laboratory ELab

Murilo Pilon Pessatti - CEO

Inovação de Produtos com Projeto de Circuitos Integrados e Casos de Sucesso

São Paulo, 29/03/11

Agenda



Case

A/D& D/A

Chipus

Power System

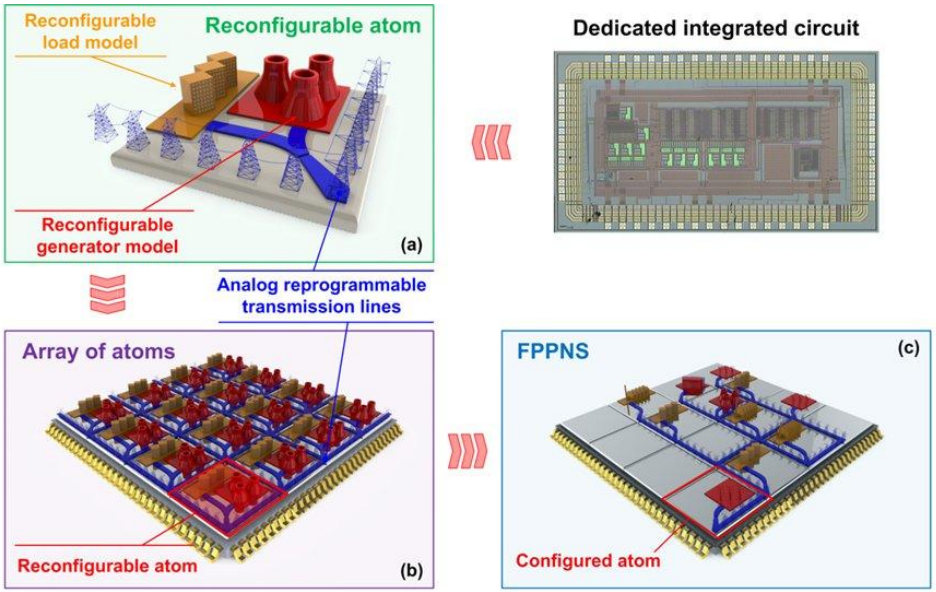
Smart Grid

Emulation

Case

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE
Electronics Laboratory ELab

+ chipus → **Company**



- A chip to emulate a power system
- EPFL develop the whole IC system
- Chipus developed the A/D & D/A IC sub-system

chipus
Electronics Laboratory ELab
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

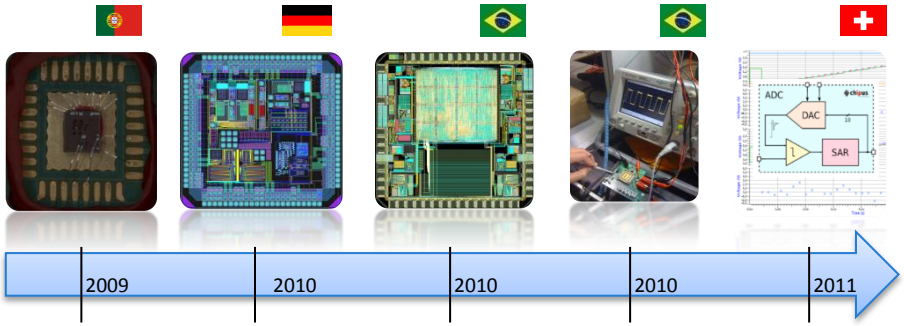
CHIPUS MICROELETRÔNICA LTDA.

“Empresa Privada, fundada em 2008, participante do CI-Brasil, especializada em projeto de circuitos integrados analógicos/mixed-signal. “

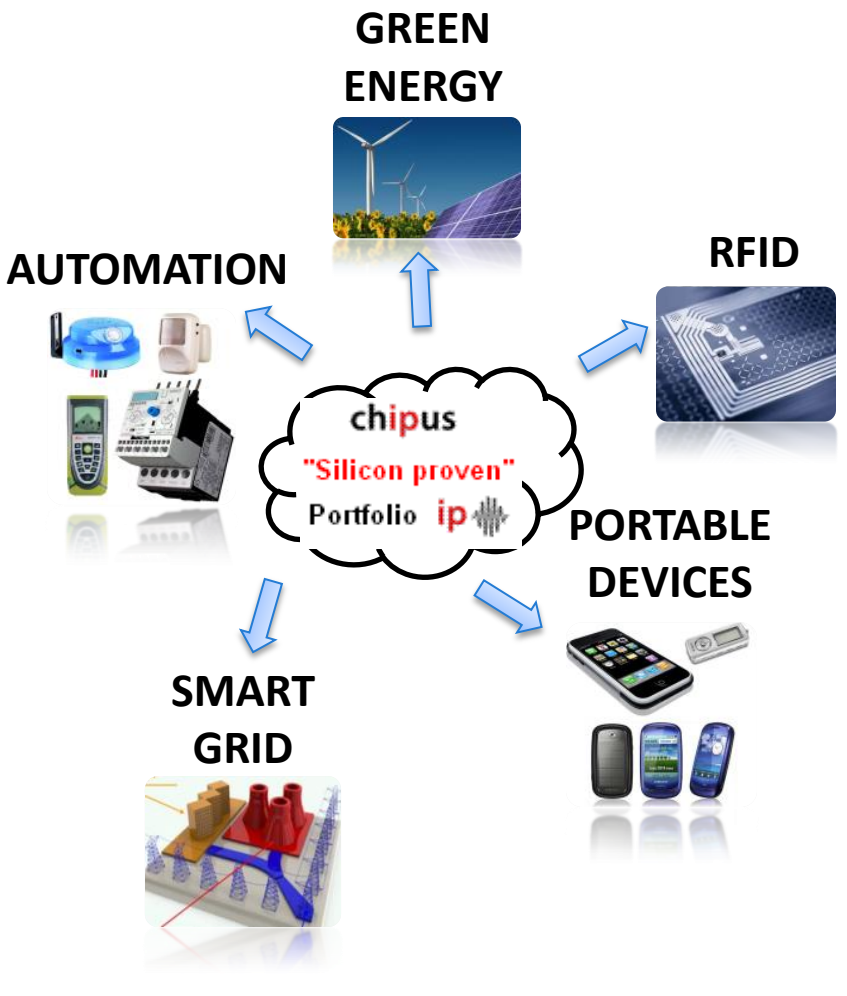
FOCO: Licenciamento de Blocos de Propriedade Intelectual (“IP”) da CHIPUS p/ empresas que desenvolvem chips.

TIME: 8 Colaboradores c/ experiência internacional, inclusive em empresas da área de semicondutores. FUJITSU CHIPIDEA

VENDAS: 1 consultor nos EUA + 1 representante China



MERCADO

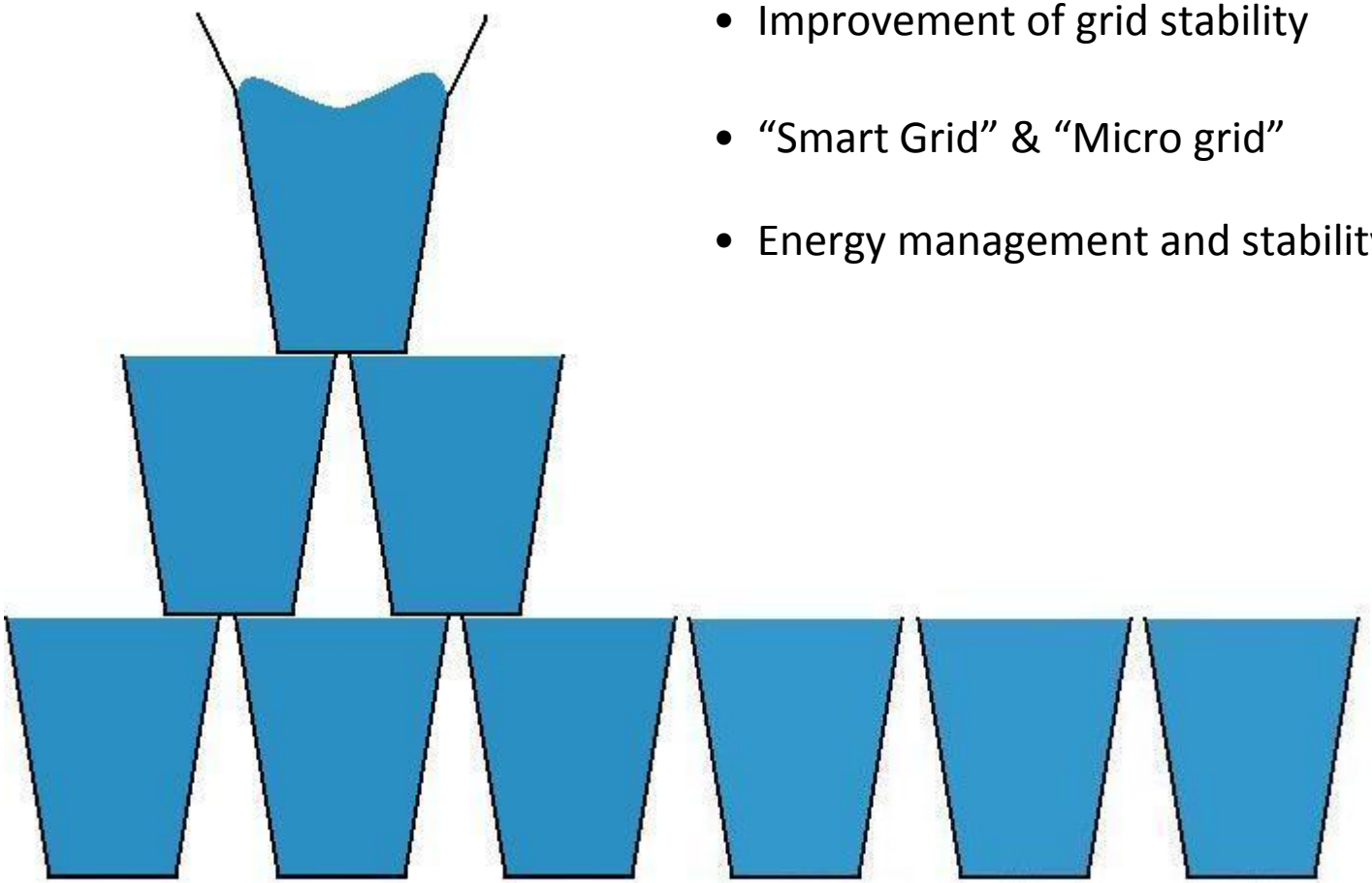


chipus

Electronics Laboratory ELab

EPFL ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Smart-Grid: Power Grid Stability

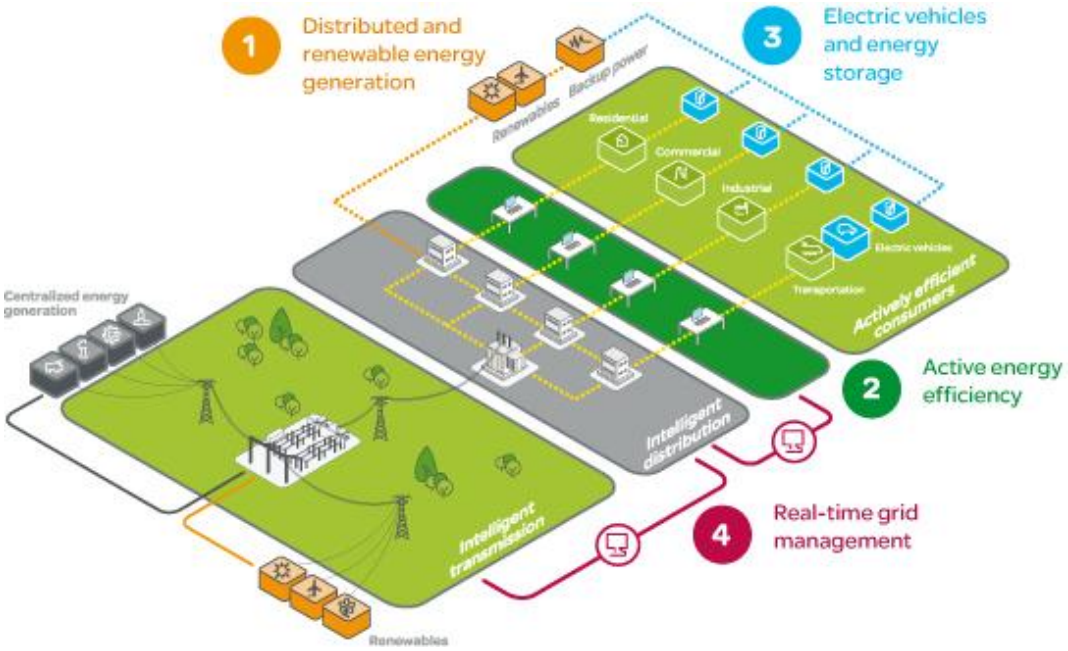


- Improvement of grid stability
- “Smart Grid” & “Micro grid”
- Energy management and stability prediction

Smart-Grid: Concept

A **smart-grid** delivers electricity from suppliers to consumers using two-way communications to control appliances at consumers' to save energy, reduce cost and increase reliability and transparency. ***It overlays the electrical grid with an information and net metering system.***

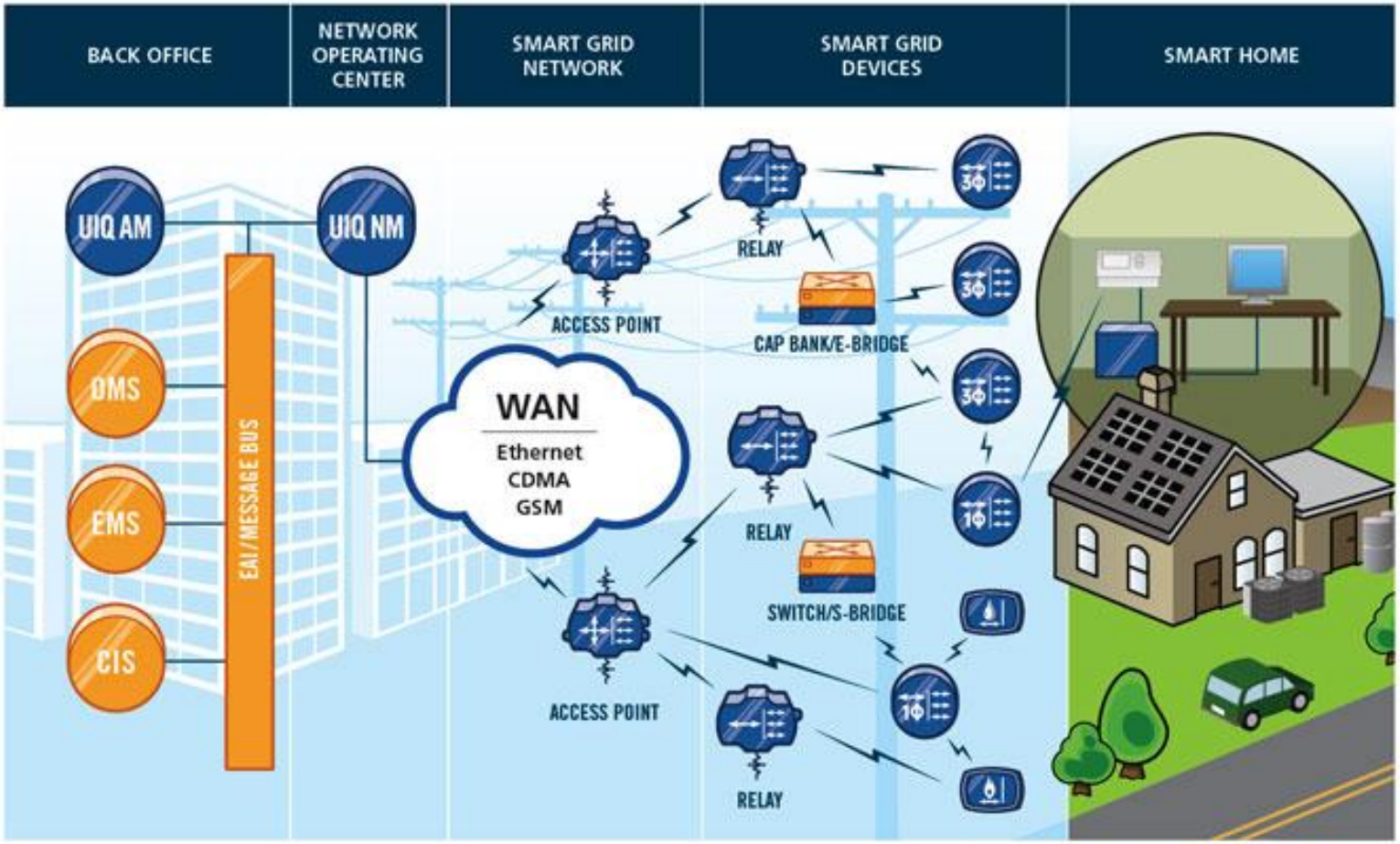
Smart-Grid: The main 4 triggers



1. **Renewable energies**, allowing consumers to be their own utilities and creating the need to connect these distributed sources to the central grid
2. **Active energy efficiency and energy management,** making energy visible and giving consumers the means to act on their energy consumption
3. **Electric vehicles**, reshaping the way everyone thinks about private and public transportation
4. **Real-time grid management**, to anticipate consumption and adapt energy accordingly

http://www.schneider-electric.com/

Smart Grid: Issues

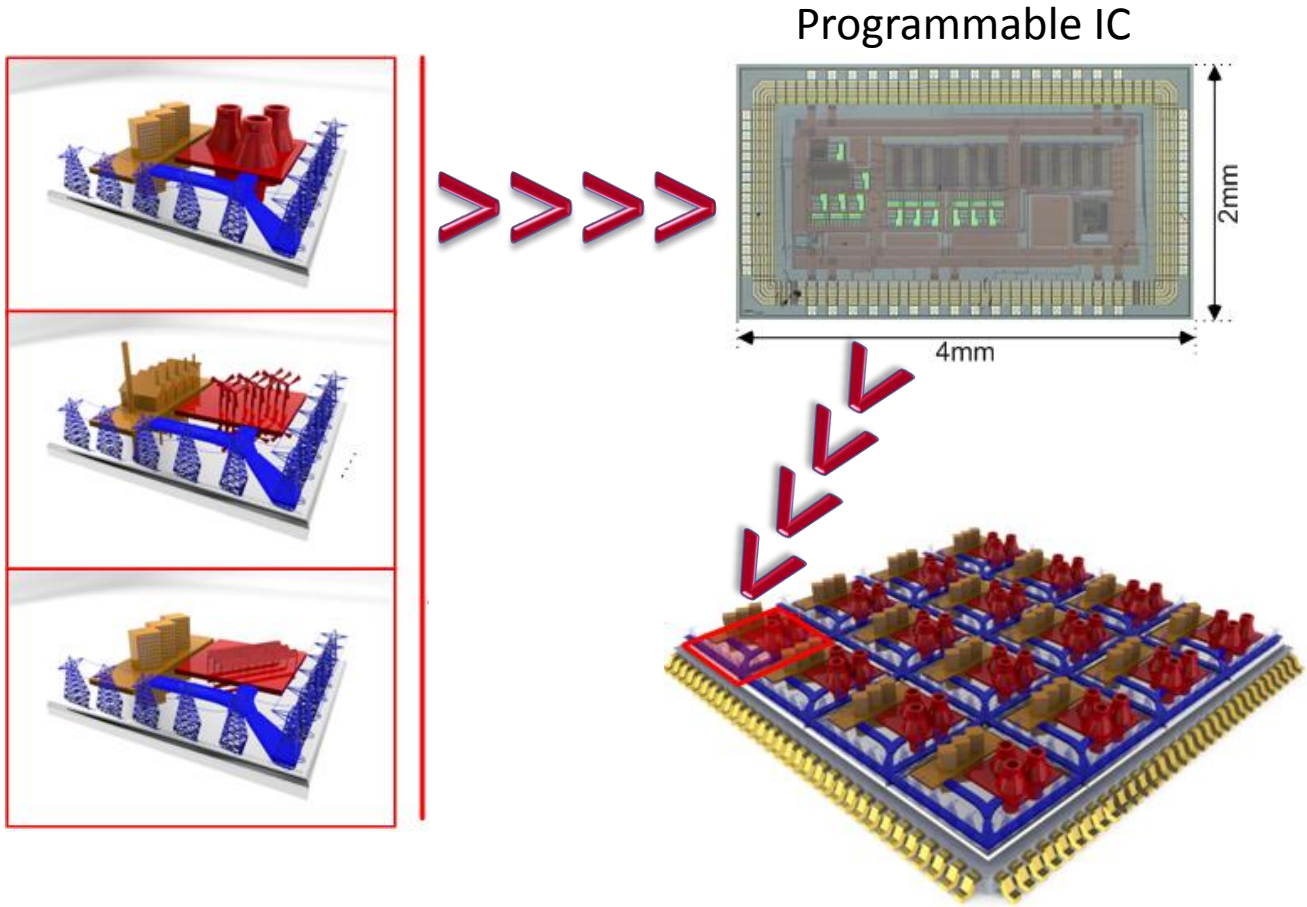


≈5 min.

Power Network Emulation:
Toward real time management Hardware

Power Network Emulation: ASIC for Smart Grid computations

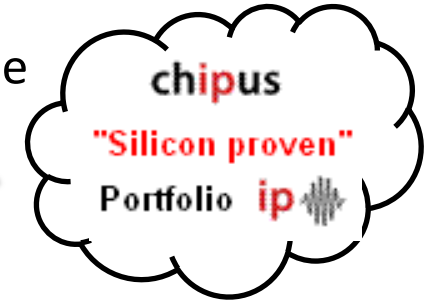
- Emulation of : load, generator & line



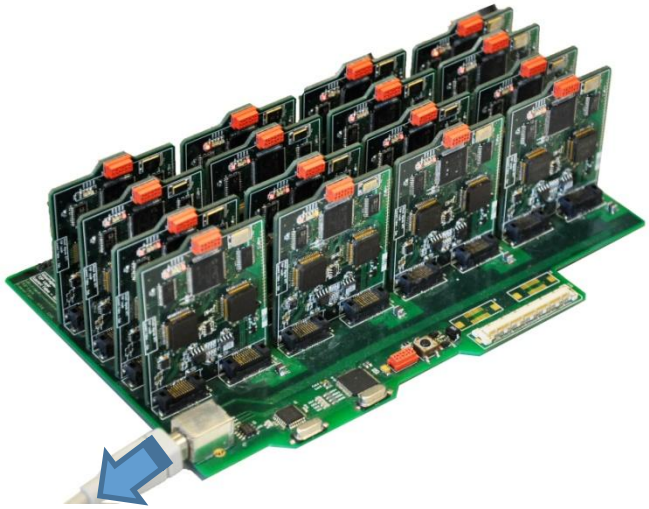
chipus
Electronics Laboratory ELab
EPFL ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Power Network Emulation: From 16 to 100 nodes

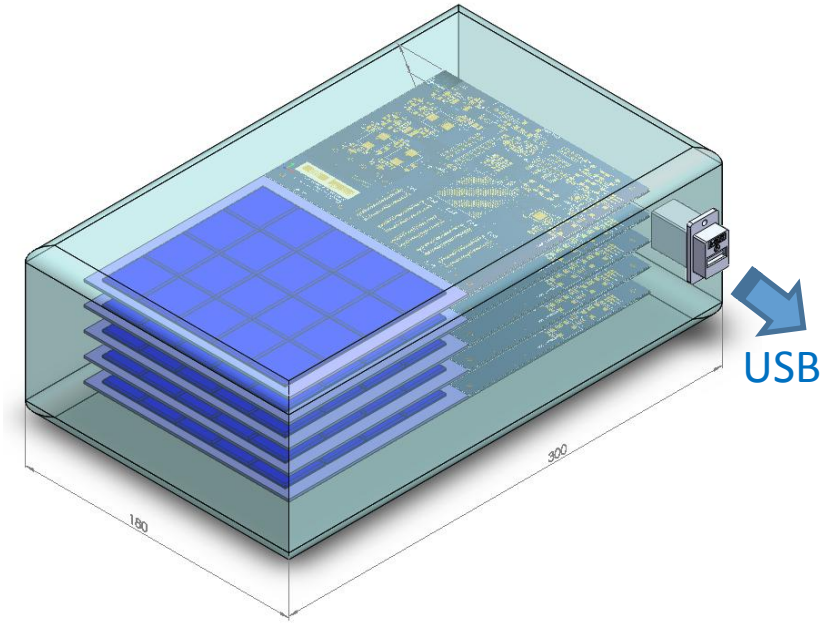
- First prototype able to emulate up to 16 nodes
- First prototype emulates up to 50-100 x faster than real time



- Next prototype targets **up to 100 nodes**
- Next prototype target **up to 1000x faster than real time**



First 16 nodes emulation prototype



Next 100 nodes emulation prototype

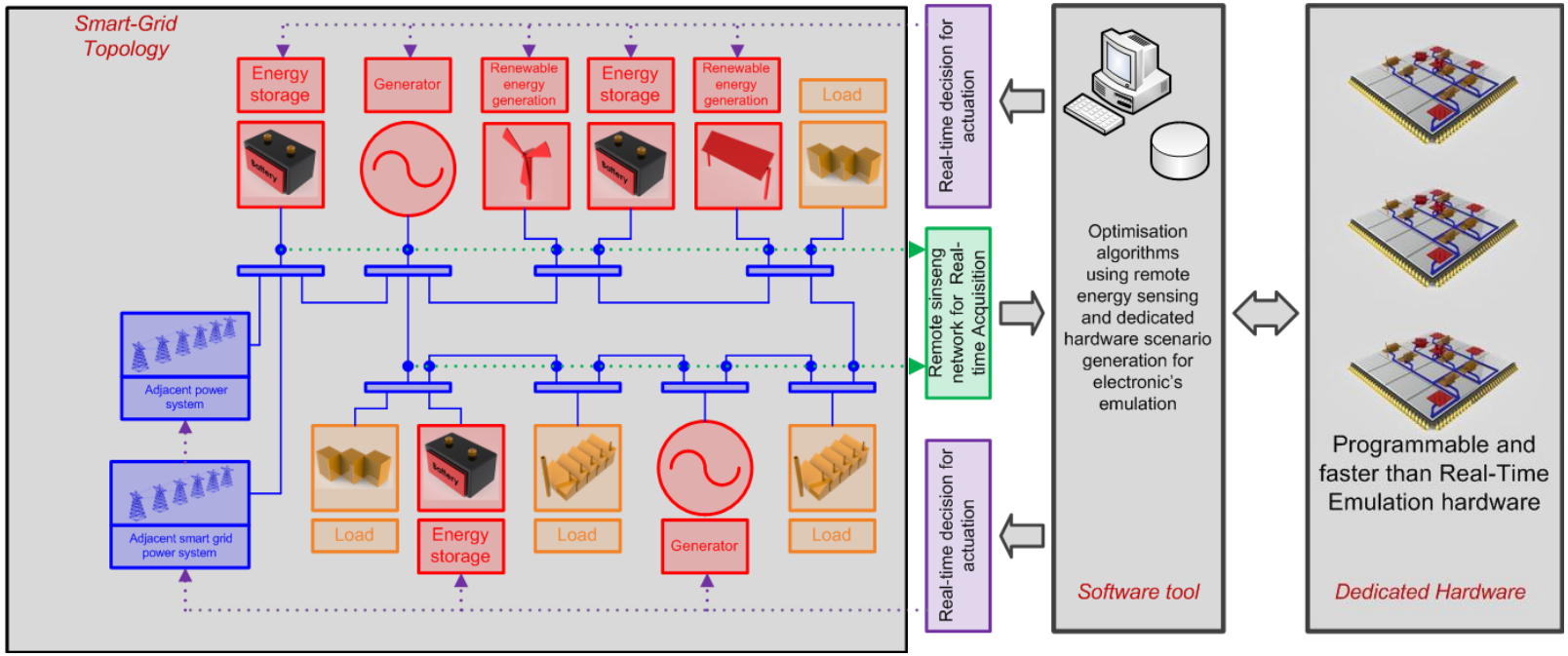
chipus

Electronics Laboratory ELab

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Power Network Emulation: Management

- Real-Time Optimization of Smart-grid



Implementation: United Arab Emirates (UAE)

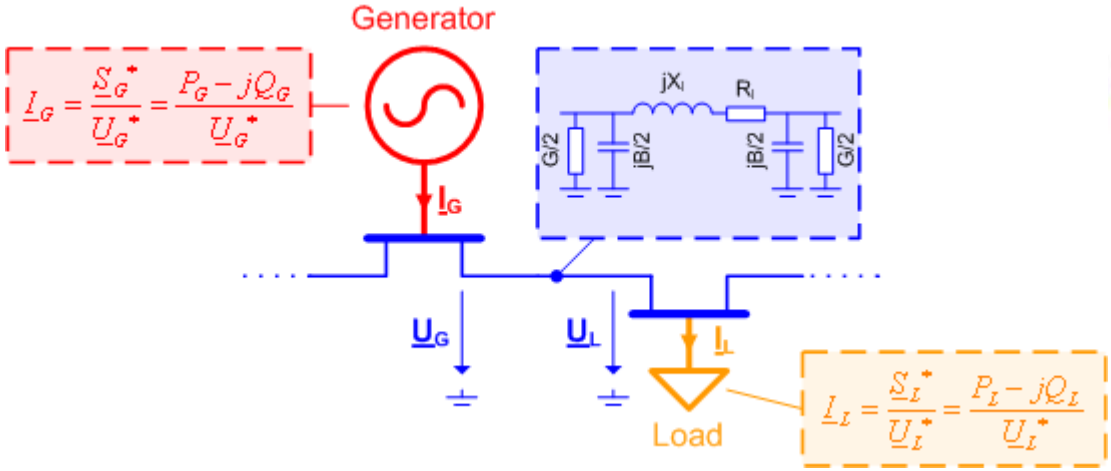
chipus

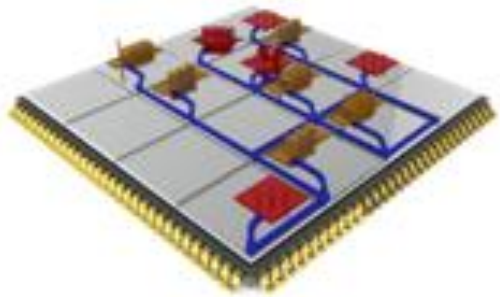
Electronics Laboratory ELab

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

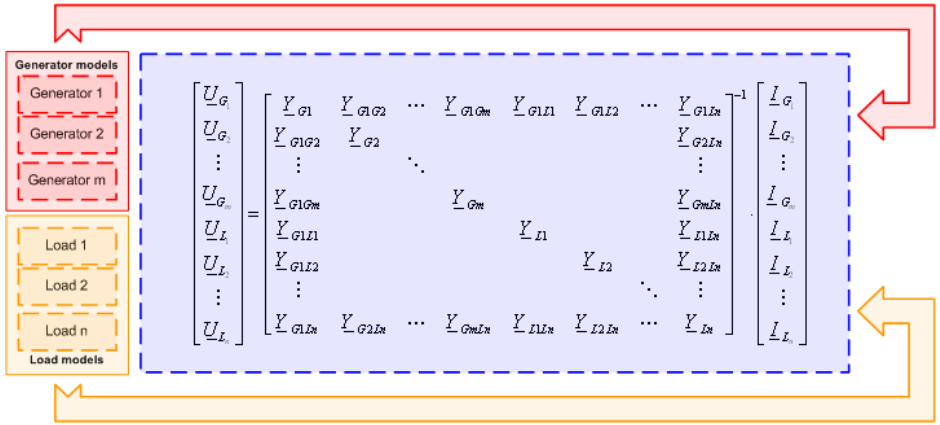
Power Network Emulation: Digital vs. Analog

- Generators + loads + grid topology

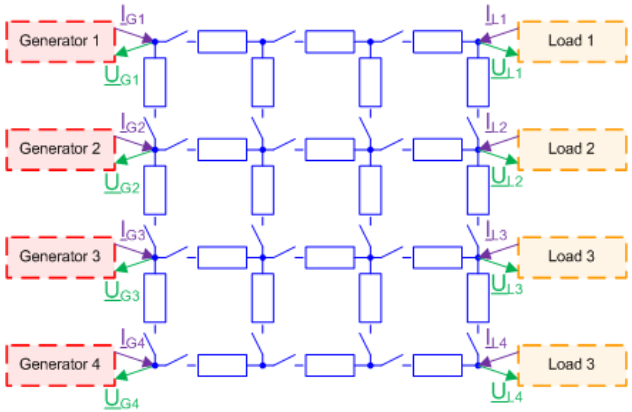




- Power system computation scheme (digital vs analog)



I_{node} » GRID MATRIX » U_{node} » node model = f(I_{node}, U_{node})



I_{node} » EMULATION » U_{node} » node model = f(I_{node}, U_{node})

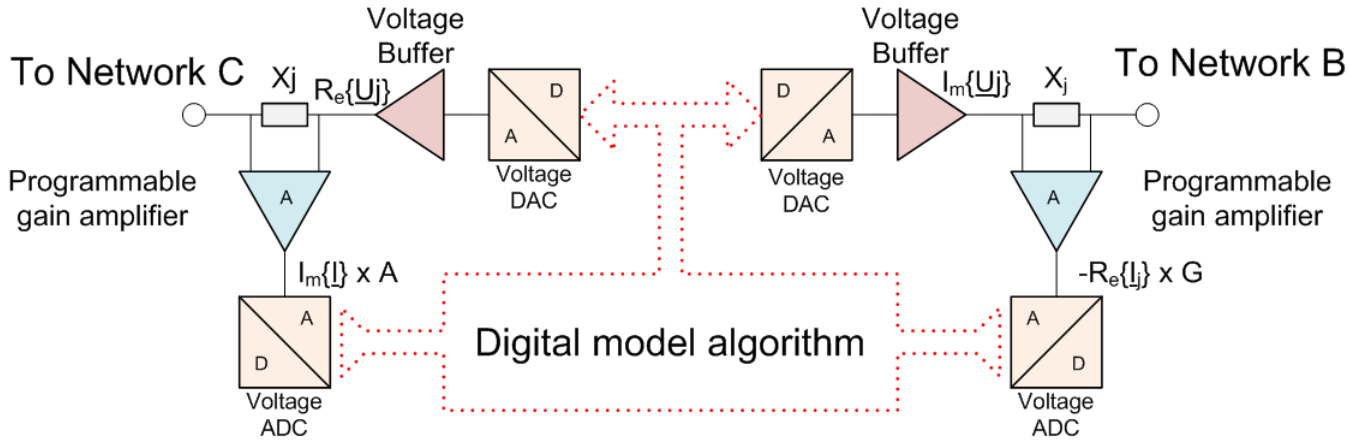
chipus

Electronics Laboratory ELab

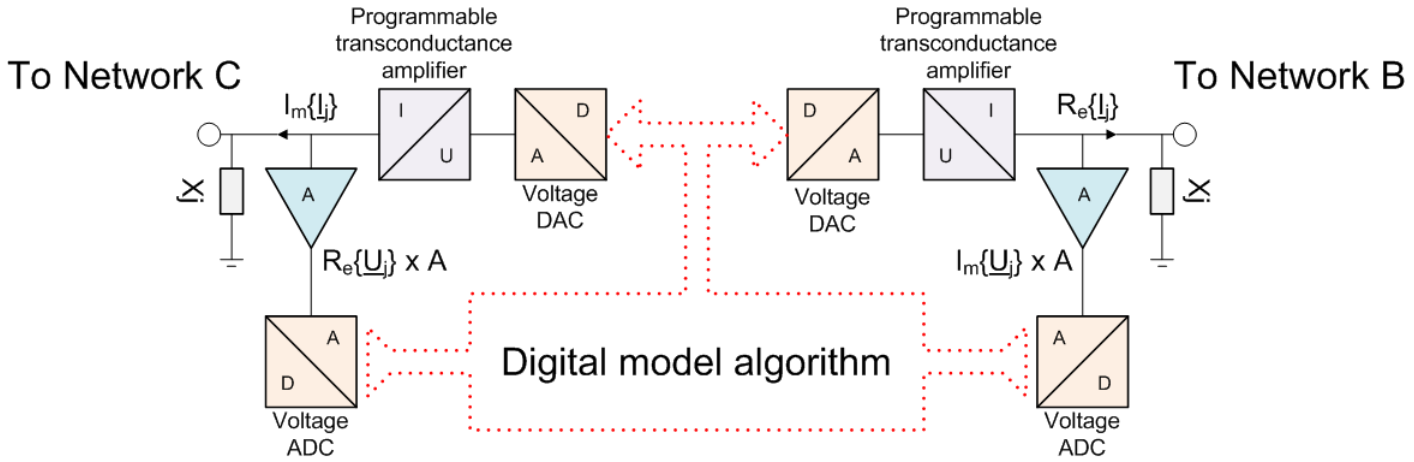
EPFL ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

Power Network Emulation: Approach

- Two different interfaces able to be implemented @ **each node**
- **Complex voltage interface** (phasor emulation approach)



- **Complex current interface** (phasor emulation approach)



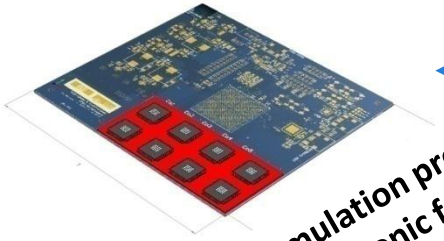
chipus

Electronics Laboratory ELab

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

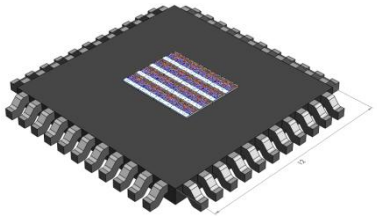
Power Network Emulation: 100 nodes in-a-chip

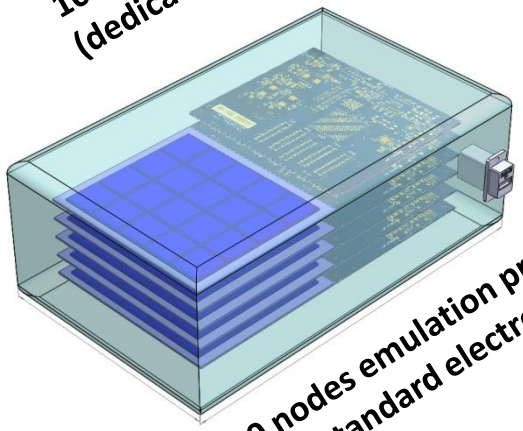
- Miniaturization of electronics functions
- Increase of the number of node by means of increase of signal-on-noise ratio
- Decrease of the price per node
- Targets: +100 nodes up to 1000 times faster than real time & 1 node / mm^2



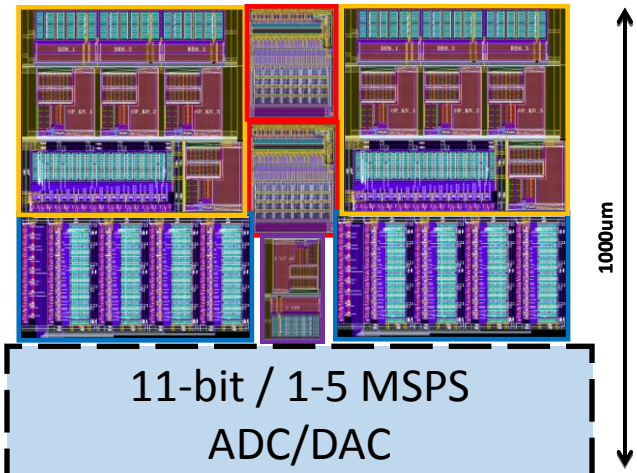
100 nodes emulation prototype (dedicated electronic functions)

100 nodes on-a-chip





100 nodes emulation prototype (standard electronic)



Floorplan of an integrated node

chipus

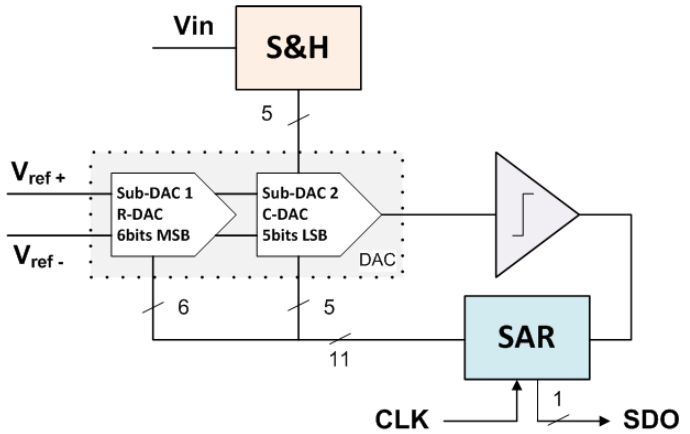
Electronics Laboratory ELab

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

11 bits / 1-5 MSPS HYBRID SAR ADC / DAC

Features

- Successive Approximation Register Analog-to-Digital Converter
- 11-bit / 1-5MSPS
- End of conversion indicator
- No missing code
- AMS 0.35um CMOS process
- Power consumption: < 5mW
- Core area: 0.15mm^2



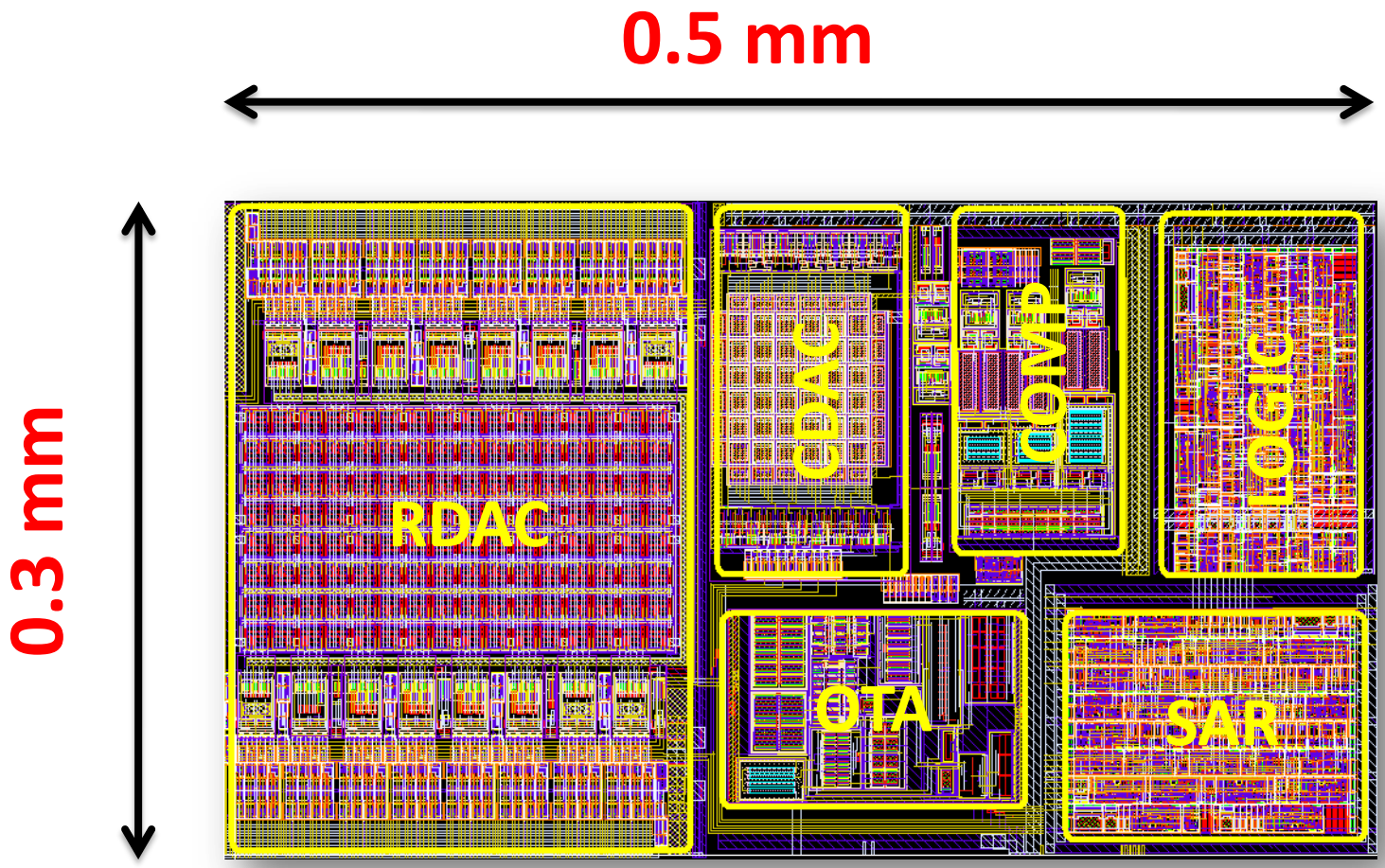
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
avdd	Analog power supply	2.7	3.3	3.6	V
dvdd	Digital power supply	2.7	3.3	3.6	V
temp	Temperature range	-40	27	125	°C
INL	Integral non-linearity	-	±0.9	±2.0	LSB
DNL	Differential non-linearity	-	±0.9	±1.0	LSB
Vos	Input offset voltage		±0.5	±2.0	LSB
Vref+	High reference voltage	1	-	3.3	V
Vref-	Low reference voltage	0	-	2	V
fclk	Clock frequency	12	-	50	MHz
t_1	Soc signal duration	-	2	-	Clock
t_{conv}	Conversion time	-	12	-	Clock
V_{in}	Analog input voltage range	Agnd+0.2	-	Avdd-0.2	V

chipus

Electronics Laboratory ELab

EPFL ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

11 bits / 1-5 MSPS HYBRID SAR ADC / DAC



chipus

Electronics Laboratory ELab

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

OBRIGADO

chipus

Chipus Microelectronics

www.chipus-ip.com

Rua Lauro Linhares, 589 – Sala 04 – 3º Andar
Trindade – FLORIANÓPOLIS – CEP 88.036-001
BRASIL
www.chipus-ip.com

Tel. +55 48 2107 2740
+55 48 9167 8067

chipus@chipus-ip.com

Electronics Laboratory
ELab

ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

murilo.pessatti@chipus-ip.com

chipus
Electronics Laboratory
ELab
ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE